AMENDMENTS TO THE CLAIMS

1. (Original) An image processor comprising:

a graphics pipeline including a first plurality of stages configured to process a graphic object,

a bit map image pipeline including a second plurality of stages configured to process a bit-mapped image, and

a selectively configurable interconnection matrix defining an image path for providing selected outputs from one or more of said stages of one of said pipelines to selected inputs of one or more of said stages of the other of said pipelines.

2. (Original) The image processor according to claim 1 wherein each of said first plurality of stages is different from the others and is selected from among the group of stages including scan conversion, clipping, windowing to viewport, projection, and sorting.

3. (Original) The image processor according to claim 1 wherein each of said second plurality of stages is different from the others and is selected from among the group of stages including demosaicing, color correction/white balancing, gamut mapping, tone correction, flare correction, color transformation, and scaling.

4. (Original) The image processor according to claim 1 further comprising an output stage connected to an output from each of said pipelines.

5. (Original) The image processor according to claim 1 wherein said interconnection comprises a switching matrix configurable to:

route outputs from one or more of said first plurality of stages to a next one of said first plurality of stages or to a selected one of said second plurality of stages; and

route outputs from one or more of said second plurality of stages to a next one of said second plurality of stages or to a selected one of said first plurality of stages.

6. (Original) The image processor according to claim 1 wherein said graphics pipeline is configured to receive graphics data including graphics identification and location data and said bit-mapped image pipeline is configured to receive a raster scanned image data representing pixel luminance information.

7. (Original) The image processor according to claim 1 further comprising a data format converter configured to convert between a graphics data format and a bit-mapped image data format.

8. (Original) The image processor according to claim 1 further comprising an image recognition stage configured to identify and encode graphic images within said bit-mapped image.

9. (Original) The image processor according to claim 1 further including a common instruction decoder operable to control said interconnection to route at least one of said graphic object and said bit-mapped image object between both said graphics and bit-mapped image pipelines.

10. (Original) A method of processing an image comprising the steps of:

selectively configuring a pipeline interconnection matrix to establish an image path through one or more stages of a graphics pipeline and one or more stages of a bit map image pipeline; and

processing an image by transmission along said image path through at least one stage of each pipeline.

11. (Original) The method according to claim 10 wherein processing performed by each of said stages of said graphics pipeline is different from processing performed by the others and is selected from among the group of processing including scan conversion, clipping, windowing to viewport, projection, and sorting.

12. (Original) The method according to claim 10 wherein processing performed by each of said stages of said bit map image pipeline is different from processing performed by the others and is selected from among the group of processing including demosaicing, color correction/white balancing, gamut mapping, tone correction, flare correction, color transformation, and scaling.

13. (Original) The method according to claim 10 further including a step of combining outputs from each of said pipelines into a merged output.

14. (Original) The method according to claim 10 wherein said step of selectively configuring said pipelines includes one of:

alternatively routing outputs from one or more stages of one of said pipelines to a next one of said stages or to a selected one of said stages of the other pipeline.

15. (Original) The method according to claim 10 wherein further including steps of passing graphics data including graphics identification and location data to said graphics pipeline and passing raster scanned image data representing pixel characteristic information to said bit map image pipeline.

16. (Original) The method according to claim 10 further comprising a step of converting between a graphics data format and a bit-mapped image data format.

17. (Original) The method according to claim 10 further comprising a step of image recognition including identification and encoding of said graphic images within said bit-mapped image.

18. (Original) The method according to claim 10 further including a step of controlling an interconnection to route at least one of said graphic object and said bit-mapped image object between both said graphics and bit map image pipelines.

19. (Original) An image processor comprising:

a first pipeline including a plurality of graphic image processors for processing a graphic object,

a second pipeline including a plurality of a bit map image processor for processing a bit-mapped image, and

a switch for selectively connecting an output from any one of said processors to an input of any other one of said processors.

20. (Original) The image processor according to claim 19 wherein:

a processing function performed by each of said graphic processors is different from a processing function performed by any other graphic processor and at least one of said processing functions is selected from among the group of processes including scan conversion, clipping, windowing to viewport, projection, and sorting; and

a processing function performed by each of said bit map image processor is different from a processing function performed by any other bit map processors, processing functions is selected from among the group of processes including demosaicing, color correction/white balancing, gamut mapping, tone correction, flare correction, color transformation, and scaling.

21. (Previously Presented) A processor comprising:

a first pipeline including a first plurality of stages configured to process a first object,

a second pipeline including a second plurality of stages configured to process a second object, and

a plurality of interconnects that connects each stage of first plurality of stages with at least one other stage in the first pipeline and with a third plurality of stages in the second pipeline, and connects each stage of second plurality of stages with at least one other stage in the second pipeline and with a fourth plurality of stages in the first pipeline.

22. (Previously Presented) The processor of claim 21 further comprising:

a converter configured to convert between a data format of the first object and a data format of the second object.

23. (Previously Presented) The processor of claim 21 further comprising:

a recognition stage configured to identify and encode the first object within the second object.

24. (Previously Presented) The processor of claim 21 further comprising:

an output stage connected to an output from each of the pipelines.

25. (Previously Presented) The processor of claim 24 further comprising:

a final stage of the first pipeline that is connected to each stage of the second plurality of stages and the output stage; and

a final stage of the second pipeline that is connected to each stage of the first plurality of stages and the output stage.